In the Claims:

1. (Cancelled)

2. (Currently Amended) A CMOS imager system comprising:

an active pixel sensor;

a column buffer connected to the active pixel sensor;

an analog-to-digital (A/D) converter co-located with the active pixel sensor and column buffer; and

~~The CMOS imager system of Claim 1, further comprising~~ an analog programmable gain amplifier connected between the column buffer and the A/D converter, such that a transmission path between the analog programmable gain amplifier and the A/D converter acts primarily as a resistance, rather than a reactance.

3. (Original) The CMOS imager system of Claim 2, wherein the active pixel sensor comprises an access supply, a tapered reset supply and a source supply.

4. (Original) The CMOS imager system of Claim 3, wherein the A/D converter is a high-speed converter have 12 bit or greater resolution.

5. (Original) The CMOS imager system of Claim 4, wherein the column buffer has gain and fixed-pattern noise (FPN) suppression.

6. (Original) The CMOS imager system of Claim 5, wherein the analog programmable gain amplifier has tunable electronic bandwidth.

7. (Original) A digital video system comprising:

an active pixel sensor;

a column buffer connected to receive an output from the active pixel sensor;

an analog programmable gain amplifier connected to the column buffer;

an analog-to-digital (A/D) converter connected to the analog programmable gain amplifier and co-located with the active pixel sensor, column buffer and analog programmable gain amplifier, such that a transmission path between the analog gain amplifier and the A/D converter acts primarily as a resistance, rather than a reactance;

a digital programmable gain amplifier connected to an output of the A/D converter; and

a digital video interface connected to an output of the digital programmable gain amplifier.

8. (Original) The digital video system of Claim 7, wherein the active pixel sensor comprises an access supply, a tapered reset supply and a source supply.

9. (Original) The digital video system of Claim 8, wherein the A/D converter is a high-speed converter have 12 bit or greater resolution.

10. (Original) The digital video system of Claim 9, wherein the column buffer has gain and fixed-pattern noise (FPN) suppression.

11. (Original) The digital video system of Claim 10, wherein the analog programmable gain amplifier has tunable electronic bandwidth.

12. (New) A CMOS imager system comprising:

an active pixel sensor;

a column buffer connected to the active pixel sensor; and

a high-speed analog-to-digital (A/D) converter, the A/D converter having greater than or equal to 12 bit resolution, co-located with the active pixel sensor and supporting multiple column buffers, such that a transmission path between the column buffers and the A/D converter acts primarily as a resistance, rather than a reactance.

13. (New) The CMOS imager system of Claim 12, further comprising an analog programmable gain amplifier connected between the column buffer and the A/D converter, such that a transmission path between the analog programmable gain amplifier and the A/D converter acts primarily as a resistance, rather than a reactance.

14. (New) The CMOS imager system of Claim 13, wherein the active pixel sensor comprises an access supply, a tapered reset supply and a source supply.

15. (New) The CMOS imager system of Claim 14, wherein the column buffer has gain and fixed-pattern noise (FPN) suppression.

16. (New) The CMOS imager system of Claim 15, wherein the analog programmable gain amplifier has tunable electronic bandwidth.